REMARKS

Claims 1 – 24 are pending. Claims 14, 16, 20 and 24 are currently amended.

Claims 14, 16, 20 and 24 were rejected under 35 U.S.C. §112 as being indefinite, because it was not clear whether a capacitor was being claimed (thus, two electrodes) or whether a single electrode was being claimed. The Office Action further noted that the language of these claims was somewhat confusing and the grammar was incorrect.

Applicants have amended claims 14, 16, 20 and 24 to address these rejections. Accordingly, Applicants respectfully request reconsideration and withdrawal of these rejections.

Claims 1, 5, 6 and 8 – 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of U.S. Patent No. 5,834,797 (Yamanaka). Applicants respectfully disagree with these rejections.

The "Background of the Invention" section of the present application discloses a first gate electrode 11, a gate insulating film 12, and a semiconductor film 13 that is formed on the gate insulating film 12. The semiconductor film 13 has a channel 13c. An insulating film (various reference numbers, for example, 12, 15, 17) is also disclosed. A display electrode 19 is connected to a source 13s that is formed in the semiconductor film 13.

The Yamanaka patent discloses an active layer 4 disposed between a first gate electrode G1 and a second gate electrode G2.

Neither the "Background of the Invention" section of the present application nor the Yamanaka patent disclose or suggest a display electrode being elongated so as to extend above a channel of a thin film transistor wherein a second gate electrode is formed between a first gate electrode and said display electrode, as recited by claim 1. Referring, for example, to figure 2, display electrode 19 is elongated to extend above channel 13c. A second gate electrode 70 is formed between a first gate electrode 11 and the display electrode 19.

A display device incorporating features recited in claim 1 may have one or more of the following advantages. Uniformity of brightness across a screen of the display device may be improved. Additionally, certain screen defects, such as bright spots, may be reduced.

Claim 1 should be allowable for at least the foregoing reasons.

Claims 5, 6 and 8 – 13 depend from claim 1 and should be allowable for at least the same reasons as claim 1.

Claims 21 –23 also were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of the Yamanaka patent. Applicants respectfully disagree.

Claim 21 recites a "display electrode being extended above [a] channel region of [a] thin film transistor; an electrode provided between the channel region of the thin film transistor and the display electrode, wherein a gate voltage is applied to the electrode." For similar reasons as discussed above with reference to claim 1, claim 21 also should be allowable.

Claims 22 and 23 depend from claim 21 and should be allowable for at least the same reasons as claim 21.

Claim 7 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art and the Yamanaka patent as applied to claims 1, 5, 6, 8 – 13 and 21 – 23 (discussed above), and in further view of U.S. Patent No. 6,100,954 (Kim et al.). Applicants respectfully disagree with this rejection. Claim 7 depends from claim 1. None of the asserted references discloses or suggests a "display electrode being elongated so as to extend above [a] channel of [a] thin film transistor . . . wherein a second gate electrode [is] formed between [a] first gate electrode and said display electrode," as recited by claim 1. Claim 7, therefore, should be allowable for at least that reason.

Claim 14 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art and the Yamanaka patent as applied to claims 1, 5, 6, 8 – 13 and 21 – 23 (discussed above), and in further view of U.S. Patent No. 5,251,049 (Sato et al.). Applicants

respectfully disagree with this rejection. Claim 14 depends from claim 1. None of the asserted references discloses or suggests a "display electrode being elongated so as to extend above [a] channel of [a] thin film transistor . . . wherein a second gate electrode [is] formed between [a] first gate electrode and said display electrode," as recited by claim 1. Claim 14, therefore, should be allowable for at least that reason.

Claim 24 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art and the Yamanaka patent as applied to claims 1, 5, 6, 8 – 13 and 21 – 23 (discussed above), and in further view of U.S. Patent No. 5,251,049 (Sato et al.). Applicants respectfully disagree with this rejection. Claim 24 depends from claim 21. None of the asserted references discloses or suggests a "display electrode being extended above [a] channel of [a] thin film transistor; an electrode provided between the channel region of the thin film transistor and the display electrode, wherein a gate voltage is applied to the electrode," as recited by claim 21. Claim 24, therefore, should be allowable for at least that reason.

Claims 2 – 4 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over the "Background of the Invention" section of the present application in view of U.S. Patent No. 5,702,963 (Vu et al.). Applicants respectfully disagree.

First, in asserting these rejections, the Office Action interpreted lines 4 – 8 of page 4 in the "Background of the Invention" section as an admission by the applicant that the prior art includes a "display electrode being elongated so as to extend above said channel of said thin film transistor" as recited, for example, by claim 2. That interpretation is incorrect. The cited passage merely contrasts certain claimed features of the present application with the prior art liquid crystal display (LCD) of figure 9.

The Vu et al. patent discloses a double gate MOSFET device 1051 with a channel region 1062. (See figures 15E and 15G) A first gate electrode G1 is positioned above the channel region 1062 and a second gate electrode G2 is positioned below the channel region 1062. The first gate electrode G1 is electrically connected to the second gate electrode G2.

Neither the prior art disclosed "Background of the Invention" section of the present application nor the Vu et al. patent discloses or suggests "a second gate electrode formed between [a] first gate electrode and [a] display electrode" as recited by claim 2. Such an arrangement is shown, for example, in figure 2 where a second gate electrode 70 is formed between a first gate electrode 11 and a display electrode 19. Claim 2 should be allowable for at least these reasons.

Claim 3, 4 and 15 depend from claim 2 and, therefore, should be allowable for at least the same reasons as claim 2.

Claims 17 – 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over the "Background of the Invention" section of the present application in view of U.S. Patent No. 5,702,963 (Vu et al.). Applicants respectfully disagree with these rejections.

Claim 17 should be allowable because, as discussed above, the Office action incorrectly interpreted lines 4 – 8 of page 4 in the "Background of the Invention" section as an admission by the applicant that the prior art includes a "display electrode being extended above [a] channel region of [a] thin film transistors" as recited by claim 17. Additionally, neither the prior art disclosed in the "Background of the Invention" section of the present application nor the Vu et al. patent discloses or suggests "a display electrode connected to one of a source region . . . and a drain region . . ., said display electrode being extended above the channel region," as recited by claim 17.

Claims 18 and 19 depend from claim 17 and, therefore, should be allowable for at least the same reasons as claim 17.

Claims 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art and the Vu patent as applied to claims 2 – 4, 15 and 17 - 19 (discussed above), and in further view of U.S. Patent No. 5,251,049 (Sato et al.). Applicants respectfully disagree with this rejection. Claim 16 depends from claim 2. None of the asserted references discloses or suggests, "a second gate electrode formed between [a] first gate electrode and [a] display

electrode" as recited by claim 2. Claim 16, therefore, should be allowable for at least that reason.

Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art and the Vu patent as applied to claims 2 – 4, 15 and 17 - 19 (discussed above), and in further view of U.S. Patent No. 5,251,049 (Sato et al.). Applicants respectfully disagree with this rejection. Claim 20 depends from claim 17. None of the asserted prior art references disclose or suggest a "display electrode being extended above [a] channel region of [a] thin film transistor" as recited by claim 17. Claim 20, therefore, should be allowable for at least that reason.

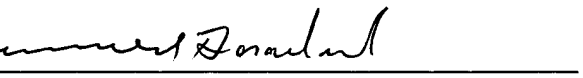
Claims 1 –24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 24 of U.S. Patent No. 6,724,011. A terminal disclaimer is enclosed to overcome the obviousness-type double patenting rejection.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a check for $130.00 for the required fee. However, please apply any additional charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: January 5, 2005



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